DESIGN Of HYBRID LOGIC 4-bit COMPARATOR With EFFICIENT VLSI DESIGN CONSTRAINTS

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Abstract: *In this paper, hybrid XOR logic is proposed to design the equality circuit. Hybrid BWIN cell is designed for knowing the status of each bit. Three levels of logic is needed to design the comparator, But with internal hardware optimized at those levels. CMOS logic is also employed for certain portion of the logic. Inverted logic is used for designing XOR, BWIN cell. In this paper the proposed comparator has been designed by using 0. 25 um implementation technology and the tool being used is Tanner tool. It has been reported that 33.5 % reduction in power was seen for the proposed design with the conventional one. 25.5% improvement in the Delay was also achieved for the proposed design when compared to the conventional design. 21% of the area benefit was there for the proposed in comparison to the existing. Power delay product has reported 55.5% efficiency for the proposed one in comparison.*

Keywords: **Hybrid Logic, Comparator, Constraints, VLSI.**

1. INTRODUCTION

Design used PTL which suffers from lack of full noise margins as in [1]. Design takes huge transistor count and it will effect the cost constraint as in [2]. Design employed carry look ahead logic to achieve high speed with low cost as in [3]. Design used pseudo logic and PTL which suffers from few drawbacks as in [4]. Design used several logic styles like PTL, TG, Pseudo, CMOS with each having their merits and demerits as in [5]. Design used full adder to satisfy the logic for the comparator as in [6]. Design used GDI technique which suffers from several drawbacks as in [7].Design has poor performance with the delay although it is functionally correct as in [8].

2. LITERATURE REVIEW[9]

4-bit Comparator has been designed by using XOR/XNOR and transmission gates. They have chosen to design AGB(A>B), ALB(A<B) and then complemented logic of OR gate can accomplish AEB(A=B). Vast use of TG(Transmission gate) ensure full swing at both the outputs. Critical path estimation is shown in the below tableI

Table I. Critical Path

S.No	Out	Level1	Level2	Level3
1	AGB	XOR,NOT	3(TG)	2(NOT)
2	ALB	XOR,NOT	3(TG)	2(NOT)

Table I shows the critical path delay estimation for AGB and ALB. To produce the output for AGB, ALB it needs 8 transistors. Three TG's in the series degrades the speed and to compensate that , non-inverting buffer is used at the end side of both the outputs.Number of devices and types of devices used are shown in the below tableII.

Table III. Hardware Used

S.No	Device	Count	Transistors	Total count
1	XOR/ XNOR	3	42	86
2	TG	18	36	
3	NOT	4	8	

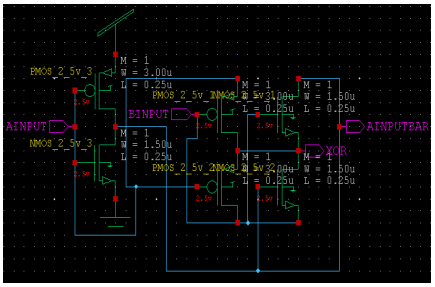
3. PROPOSED COMPARATOR

Comparator design needs any of the two out of three possible outputs. The choice depends on the designer way of thinking. We have chosen to design AEB(A=B), ALB(A<B) and then complemented logic of OR gate can accomplish AGB(A>B).

3.1 XOR CELL

The XOR cell is needed at every bit position of A and B to know the status of AEB. It is also required to design ALB, where every bit position of A and B needs to be tracked except the least significant part. XOR is designed with hybrid logic and it also ensures complete swing between the power rails. Six transistors are needed to design XOR and it produces two outputs. They are inverted logic of A and XOR. Fig.3.1.1 shows a XOR logic where P-MOSFET drives logic'1' and N-MOSFET drives logic'0'.

3.1.1. XOR CELL



The logic of XOR says that when A is '0' then output should be B, similarly when B is '0' then output should be A.when A is '1' then B' and this much amount of logic satisfys the logic of XOR. This way of understanding the logic has few limitations like lack of complete noise margins. The below tableIII shows the logical correctness along with the full swing. The first row logic leads to the full swing for "01" input combination and in the similar way the other rows will lead to the full swing for the rest of the input combinations.

Table IIIII. XOR Full Swing

S.No	Input	Logic	Full Swing
1	A=0	Out=B	01
2	B=0	Out=A	10
3	B=1	Out=A'	11
4	A'=1	Out=B	00

The below tableIV shows the transistors which are on to generate the output for the possible input combinations. Critical path delay is for “00” input combination, where one PMOS and one NMOS needs to be on to produce ‘0’.

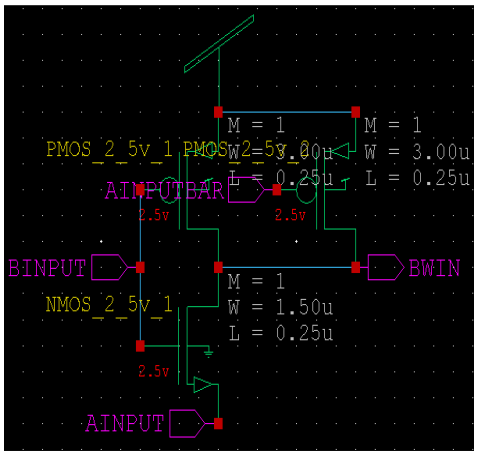
Table IV. XOR Path

S.No	Ainput,Binput	Path(Output)
1	00	P3N2(0)
2	01	P2(1)
3	10	P1(1)
4	11	N3N1(0)

3.2. BWIN CELL

The BWIN cell is needed for every bit position of A and B to know the status of ALB. BWIN cell is designed with hybrid logic and it also ensures complete swing between the power rails. Three transistors are needed to design BWIN cell, since inverted logic of A is produced by XOR cell. and it produces one output . Fig.3.2.1 shows a BWIN cell logic where P-MOSFET drives logic’1’ and N-MOSFET drives logic’0’.

3.2.1. BWIN CELL



The logic of BWIN says that when A is ‘0’ then output should be B’, when A is ‘1’ then ‘1’ to produce inverted logic of ALB. This much amount of logic satisfys the logic of BWIN. This way of understanding the logic has few limitations like lack of complete noise margins. The below tableV shows the logical correctness along with the full swing. The third row logic leads to the full swing for “01” input combination and in the similar way the other rows will lead to the full swing for the rest of the input combinations.

Table V. BWIN Full Swing

S.No	Input	Logic	Full Swing
1	A’=0	Out=1	10,11
2	B=0	Out=1	10,00
3	B=1	Out=A	01

The below tableVI shows the transistors which are on to generate the output for the possible input combinations. Critical path delay is for “11” input combination, where one NMOS and one PMOS needs to be on to produce ‘1’.

Table VI. BWIN Path

S.No	Ainput,Binput	Path(Output)
1	00	P1(1)
2	01	N1(0)
3	10	P1,P2(1)
4	11	P2,N1(1)

3.3. 4-BIT BWIN CELL

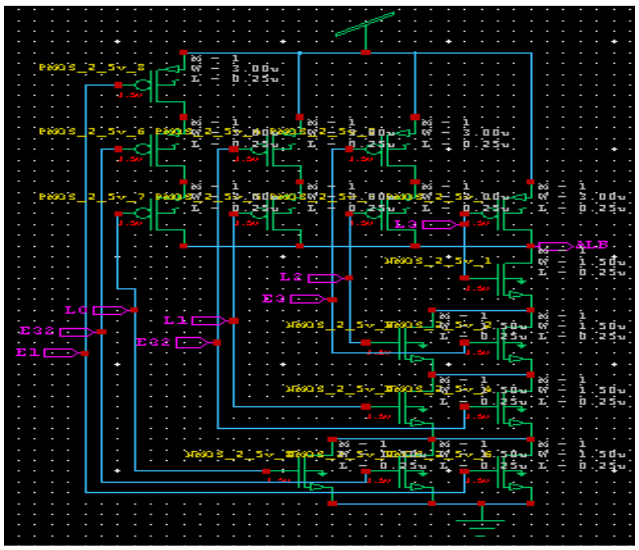
To design 4-bit BWIN cell, there will be four conditions to produce the output of logic'1'. Logic details are shown in the below tableVII.

Table VII. 4-Bit BWIN cell logic

S.No	Inputs	Input	Path (Output)
1	A3,B3=01	L3=0	L3,P(1)
2	A2,B2=01,A3XOR B3	L2,E3=0	L2,E3,P(1)
3	A1,B1=01,A3XOR B3, A2 XOR B2	L1,E32=0	L1,E32,P(1)
4	A0,B0=01,A3 XOR B3, A2 XOR B2, A1 XOR B1	L0,E32, E1=0	L0,E32, E1,P(1)

The logic is produced with two levels, that is in the first level ALB, AEB is generated in the inverted logic. Critical path is activated by applying the test vector in the fourth row. The above logic gets transformed into pull-up network. In the pull-down network critical path comprises of four NMOSFETS as shown in the figure 3.3.1.

3.3.1. 4-BIT BWIN CELL



3.4. 4-BIT COMPARATOR

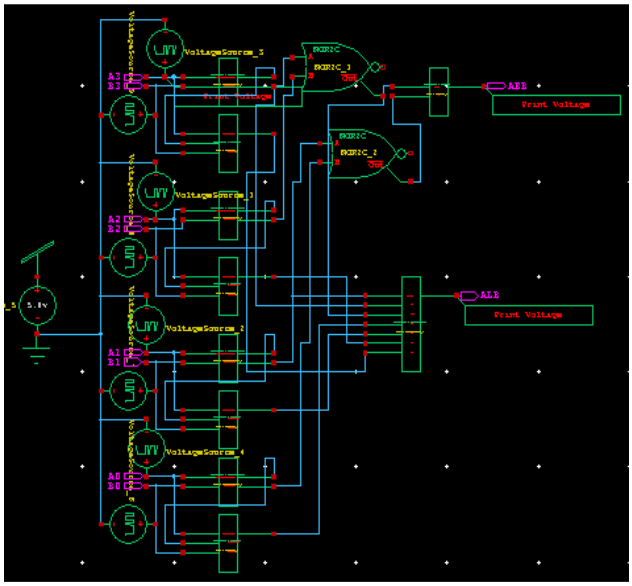
4-bit comparator is designed with AEB and ALB. AEB is generated in three levels. ALB is produced in two levels. Critical path of 4-bit comparator shown in figure 3.4.1 is mentioned in the tableVIII.

Table VIII. Critical Path

S.No	Out	Level1	Level2	Level3
1	AEB	XOR	OR	NOR
2	ALB	BWIN	4-bit BWIN	-

AEB needs 7 transistors to be on and produce the output for it's critical path. ALB requires 6 transistors to be on and produce output for it's critical path.

3.4.1. 4-BIT COMPARATOR



3.5. Hardware Analysis

Hardware analysis is used to estimate the types of components and it's quantity.

Table IX. Hardware Used

S.No	Device	Count	Transistors	Total count
1	XOR	4	24	68
2	BWIN	4	12	
3	OR	2	12	
4	4-bit BWIN	1	16	
5	NOR	1	4	

Table IX describes the types of hardware and the transistor count required to design 4-bit comparator.

4. Results

The Proposed design needs to be evaluated for the performance with the considered constraints. Delay, power and area are the constraints of our interest.

4.1. DELAY ANALYSIS

To perform the delay analysis, critical path activated input test vectors has been applied. The results in the table are based on the test vectors applied as shown in the tableX.

Table X. Test Vectors

S.No	Input Combination	Pulse Width	Rise, Fall Time
1	A3=000	10ns	0.1ns
2	B3=000	10ns	100ps
3	A2=000	10ns	0.1ns
4	B2=000	10ns	100ps
5	A1=000	10ns	0.1ns
6	B1=000	10ns	100ps
7	A0=000(101)	10ns	0.1ns
8	B0=010	10ns	100ps

All the test vectors are common for both the designs except for A0=000 for the proposed design and A0=101 for the conventional design. This is due to AEB was proposed and AGB was the conventional design.

Table XIV. Critical Path delay

S.No	Design	Delay(High,Low)ns	Delay(High,Low)ns
1	Proposed	AEB(0.27, 0.35)	ALB(0.33,0.25)
2	Existing[9]	AGB(0.36, 0.27)	ALB(0.47,0.26)

The above tableXI indicates for ALB in the proposed design , delay is 0.33ns where for the conventional one it is 0.47ns. The delay for AEB in the proposed design is 0.35, where as for the existing one AGB delay is 0.36.

4.2. POWER ANALYSIS

Power will be consumed only when the output has a event and that event should reach the supply. Activating such events in the design by applying suitable test patterns for certain duration ensures the power consumption can be estimated . The results for the proposed design are based on the tableXII shown below.

Table XII. Test Vectors

S.No	Input Combinations
1	A3=00000000000000000111111101111111
2	B3=10000000100000001111111111111111
3	A2=10000000110111110000001001011111
4	B2=00100000111111110010001011111111
5	A1=10100111101001110000011100000111
6	B1=00001111101011110000111110101111
7	A0=10111001101110010001000100010001
8	B0=00010011101110110001001110111011

The above tableXII ensures for every cycle there will be a power consuming event either for ALB or AEB.The results for the existing design are based on the tableXIII shown below.

Table XIII. Test Vectors

S.No	Input Combinations
1	A3=01000000010000000111111101111111
2	B3=10000000100000001011111110111111
3	A2=10010000110111110001001001011111
4	B2=00100000111011110010001011101111
5	A1=10100111101001110000011100000111
6	B1=00001011101010110000101110101011
7	A0=10111001101110010001000100010001
8	B0=00010010101110100001001010111010

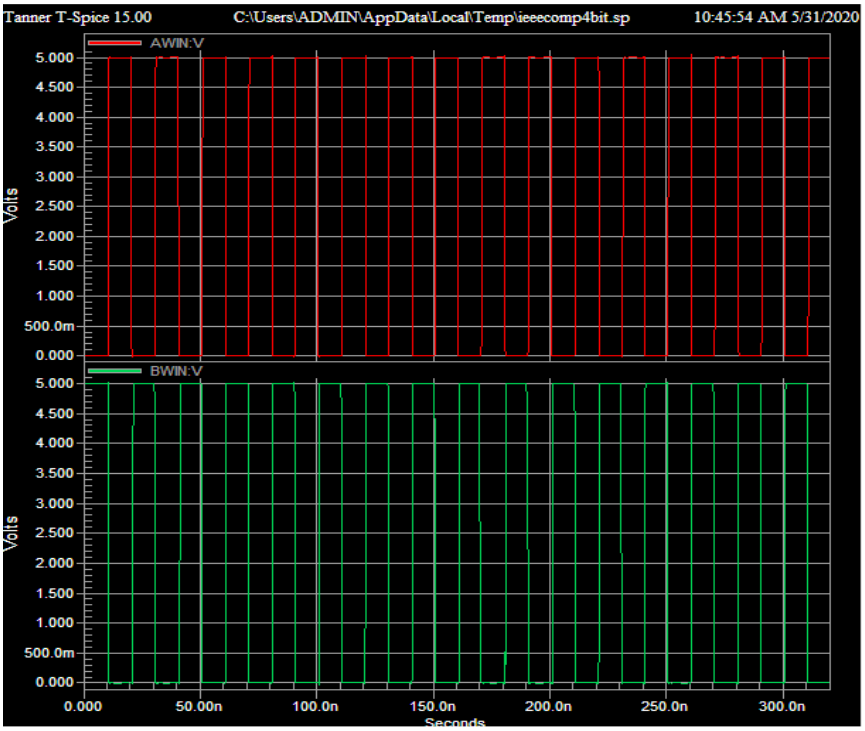
The above table ensures for every cycle there will be a power consuming event either for ALB or AGB.

Table XIV. Performance Estimation

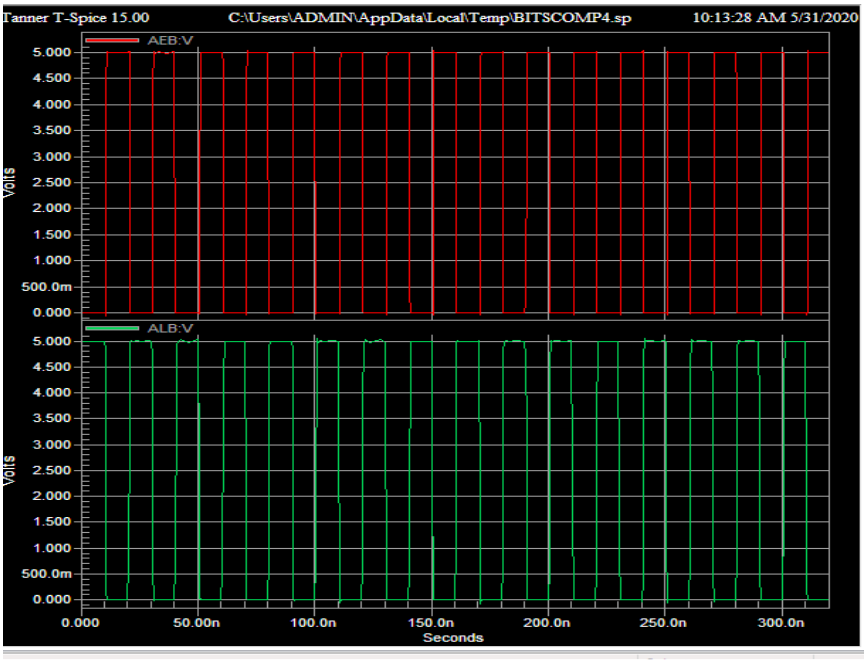
S.No	Design	Power Consumption	Delay	PDP
1	Proposed	1.124856 mw	0.35ns	0.393
2	Existing [9]	1.691054 mw	0.47ns	0.795

The above tableXIV shows there is a significant reduction in the average power consumption for the proposed design when compared to the existing design. Power simulation results are shown in the below figure 4.2.1 for the existing and 4.2.2 for the proposed one.

4.2.1 POWER RESULTS



4.2.2 POWER RESULTS



5. Conclusion

4-bit comparator has been proposed and evaluated for performance with comparison. It has been observed that 33.5% reduction in power was there for the design which we proposed. Critical path delay is for about 25.5% reduction for the proposed design. Area was saved for about 21% for the proposed design. Coming to the power delay product for about 50.5% reduction was seen for the proposed design.

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